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10/518,602	03/04/2005	Yuji Ando	U1927.0014	5070

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EXAMINER	
LANDAU, MATTHEW C	
ART UNIT	**PAPER NUMBER**
2815	

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Please find below and/or attached an Office communication concerning this application or proceeding.

H:A

Office Action Summary	Application No.	Applicant(s)	
	10/518,602	ANDO ET AL.	
	Examiner	Art Unit	
	Matthew Landau	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *36-85* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *62-85* is/are allowed.

6)☒ Claim(s) *36-61* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The drawings were received on 8/25/2005. These drawings are acceptable.

Claim Objections

Claims 36, 49, 62, 63, 71, 73, and 74 are objected to because of the following informalities: it is suggested the limitation "comprises a compound semiconductor using Ga_vAl_{1-v} (where, $0 \leq v \leq 1$) as a main component of Group III-elements and N as a main component of Group V-elements" be changed to "comprises a Group III-V compound semiconductor using Ga_vAl_{1-v} (where, $0 \leq v \leq 1$) as a main component of the Group III-elements and N as a main component of the Group V-elements" (or something similar).

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 36-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art (APA) in view of Furukawa et al. (US Pat. 4,951,121, hereinafter Furukawa).

Regarding claims 36 and 37, Figure 1 of the instant application (the APA) discloses a semiconductor device comprising a semiconductor layer 64 using GaAl as a main component of the Group III-elements and N as a main component of the Group V-elements and a Schottky junction metal layer 67 which is in contact with the semiconductor layer, wherein: said Schottky junction metal layer comprises a laminated structure wherein a first metal layer 671 is in contact with said semiconductor layer, a third metal layer 672 is above the first metal layer; and said first metal layer comprises Ni. The difference between the APA and the claimed invention is a metal layer (second metal layer) between the first and third layers comprising Mo. Figure 1 of Furukawa discloses a Schottky electrode on a III-V semiconductor layer 5, wherein the electrode comprises first, second, and third metal layers. The second metal layer 3 comprises Mo, and the third metal layer 2 comprises gold (col. 3, lines 40-50). In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to further modify the invention of the APA by including an Mo layer between the first layer 671 and the third layer 672 for the purpose of reducing the unwanted penetration of gold through the high melting metal layer into the substrate (col. 2, lines 44-47 of Furukawa). Further note that said second metal layer comprises a metal material (Mo) having a higher melting point than those of the metal materials in said first metal layer (Ni) and said third metal layer (Au), and said third metal layer comprises a metal material (Au) having a lower resistivity than those materials in said first metal layer and said second metal layer.

Regarding claims 38 and 39, in the above combination, the first metal layer comprises a material (Ni) that inherently has a higher work function than that of the metal materials in the second and third layers (Mo and Au, respectively).

Regarding claim 40, in the above combination, the material of the second metal layer is Mo. Mo has a melting point of approximately 2600 degrees C.

Regarding claims 41 and 42, Figure 1 of the APA discloses said semiconductor layer 64 is formed on a multilayered structure comprising a plurality of compound semiconductor layers formed on a sapphire substrate 1.

Regarding claim 43, Figure 1 of the APA discloses the semiconductor layer 64 is an AlGaN layer.

Regarding claims 44 and 45, Figure 1 of the APA discloses the semiconductor layer 64 is a GaN compound semiconductor (AlGaN) electron supplying layer formed on a GaN compound semiconductor (GaN) channel layer.

Claims 36, 46-49, and 59-61 are rejected under 35 U.S.C. 103(a) as being unpatentable over Teraguchi et al. (US Pat. 6,521,998, hereinafter Teraguchi) in view of Nishii et al. (US PgPub 2003/0109088, hereinafter Nishii) and Furukawa.

Regarding claims 36, 37, 49, and 50, Figure 9 of Teraguchi discloses a semiconductor device comprising a semiconductor layer 106 using Ga as a main component of the Group III-elements and N as a main component of the Group V-elements and a Schottky junction metal layer 108 (third metal layer). Note that Teraguchi discloses the third metal layer 108 is made of gold (col. 1, lines 30-34). The difference between Teraguchi and the claimed invention is a first and a second metal layer between the third metal layer 108 and the semiconductor layer 106, the first layer in contact with the semiconductor layer and the second layer in contact with the first layer, wherein the first layer comprises PdSi and the second layer comprises Mo. Figure 1 of

Nishii discloses a Schottky junction metal layer 6 over a GaN semiconductor layer 4, wherein the metal layer 6 comprises $Pd_{z3}Si_{1-z3}$ (z3=.2) (paragraph [0063]). In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of the Teraguchi by using PdSi with the above stoichiometry for the purpose of reducing electrode peeling (paragraph [0051]) while maintaining good Schottky characteristics (paragraph [0063]). Furthermore, Figure 1 of Furukawa discloses a Schottky electrode on a III-V semiconductor layer 5, wherein the electrode comprises first, second, and third metal layers. The second metal layer 3 comprises Mo, and the third metal layer 2 comprises gold (col. 3, lines 40-50). In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to further modify the invention of the Teraguchi by including an Mo layer between the first layer and the third layer 108 for the purpose of reducing the unwanted penetration of gold through the high melting metal layer into the substrate (col. 2, lines 44-47 of Furukawa). Further note that said second metal layer comprises a metal material (Mo) having a higher melting point than those of the metal materials in said first metal layer (PdSi) and said third metal layer (Au), and said third metal layer comprises a metal material (Au) having a lower resistivity than those materials in said first metal layer and said second metal layer.

Regarding claims 46, 47, 59, and 60, Figure 9 of Teraguchi discloses said semiconductor layer 106 is a GaN compound semiconductor channel layer comprising GaN formed on a GaN compound semiconductor electron supplying layer (doped layer) comprising AlGaN.

Regarding claims 48 and 61, Figure 9 of Teraguchi discloses said semiconductor layer 106 is a n-type GaN channel layer. Note that Teraguchi discloses metal layer 108 forms a

Schottky junction (col. 1, lines 26-28), and that a Schottky junction is formed only when using n-type semiconductors (col. 1, lines 35-38). Therefore, layer 106 is n-type.

Claims 49-58 are rejected under 35 U.S.C. 103(a) as being unpatentable over the APA in view of Nishii and Furukawa.

Regarding claims 49 and 50, Figure 1 of the instant application (the APA) discloses a semiconductor device comprising a semiconductor layer 64 using GaAl as a main component of the Group III-elements and N as a main component of the Group V-elements and a Schottky junction metal layer 67 which is in contact with the semiconductor layer, wherein: said Schottky junction metal layer comprises a laminated structure wherein a first metal layer 671 is in contact with said semiconductor layer, a third metal layer 672 is above the first metal layer. The difference between the APA and the claimed invention is said first metal layer comprises $Pd_{z3}Si_{1-z3}$ (where, $0.5 \leq z3 \leq 0.85$). Figure 1 of Nishii discloses a Schottky junction metal layer 6 over a GaN semiconductor layer 4, wherein the metal layer 6 comprises $Pd_{z3}Si_{1-z3}$ (z3=.2) (paragraph [0063]). Also note that the APA discloses layer 671 can be made of Pd (page 2, lines 8-10 of the instant specification). In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of the APA by using PdSi with the above stoichiometry for the purpose of reducing electrode peeling (paragraph [0051]) while maintaining good Schottky characteristics (paragraph [0063]). A further difference between the APA and the claimed invention is a metal layer (second metal layer) between the first and third layers comprising Mo. Figure 1 of Furukawa discloses a Schottky electrode on a III-V semiconductor layer 5, wherein the electrode comprises first, second, and third metal

layers. The second metal layer 3 comprises Mo, and the third metal layer 2 comprises gold (col. 3, lines 40-50). In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to further modify the invention of the APA by including an Mo layer between the first layer 671 and the third layer 672 for the purpose of reducing the unwanted penetration of gold through the high melting metal layer into the substrate (col. 2, lines 44-47 of Furukawa). Further note that said second metal layer comprises a metal material (Mo) having a higher melting point than those of the metal materials in said first metal layer (PdSi) and said third metal layer (Au), and said third metal layer comprises a metal material (Au) having a lower resistivity than those materials in said first metal layer and said second metal layer.

Regarding claims 51 and 52, in the above combination, the first metal layer comprises a material (PdSi) that inherently has a higher work function than that of the metal materials in the second and third layers (Mo and Au, respectively).

Regarding claim 53, in the above combination, the material of the second metal layer is Mo. Mo has a melting point of approximately 2600 degrees C.

Regarding claims 54 and 55, Figure 1 of the APA discloses said semiconductor layer 64 is formed on a multilayered structure comprising a plurality of compound semiconductor layers formed on a sapphire substrate 1.

Regarding claim 56, Figure 1 of the APA discloses the semiconductor layer 64 is an AlGaN layer.

Regarding claims 57 and 58, Figure 1 of the APA discloses the semiconductor layer 64 is a GaN compound semiconductor (AlGaN) electron supplying layer formed on a GaN compound semiconductor (GaN) channel layer.

Allowable Subject Matter

Claims 62-85 would be allowable if rewritten or amended to overcome the claim objections set forth in this Office action.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claims 62-73, the prior art of record, either singularly or in combination, does not disclose or suggest the combination of limitations including said first metal layer comprises any metal material selected from a group comprising Ni_yN_{1-y} and Pd_yN_{1-y} (where, $0 < y < 1$).

Regarding claims 74-85, the prior art of record, either singularly or in combination, does not disclose or suggest the combination of limitations including said first metal layer comprises any metal material selected from a group comprising $Ni_{y4}N_{1-y4}$ and $Pd_{y5}N_{1-y5}$ (where, $0.5 \leq y5 \leq 0.85$ and $0.5 \leq y4 \leq 0.85$).

Response to Arguments

Applicant's arguments filed August 25, 2005 have been fully considered but they are not persuasive.

Applicant argues that "the power increase engendered by inserting a refractory metal (Mo) layer can be achieved only in the configuration of the present invention, in which a metal having a large work function is used in the first metal layer that contacts with the GaN semiconductor, and a metal having a low resistivity is used in the third metal layer". However, the claims do not recite any limitations regarding power increase. Whether or not the

combination of the admitted prior art and Furukawa results in the aforementioned power increase has no bearing on the patentability of the claims. The fact that applicant has recognized another advantage which would flow naturally from following the suggestion of the prior art cannot be the basis for patentability when the differences would otherwise be obvious. See *Ex parte Obiaya*, 227 USPQ 58, 60 (Bd. Pat. App. & Inter. 1985). Applicant's arguments on pages 17 and 18 regarding Furukawa point out differences between the characteristics of GaN FETs and GaAs FETS. Furukawa was relied upon for teaching three layered electrode structure with a barrier layer (Mo) between a gold upper layer and a high melting point metal lower layer. Furukawa states that the barrier layer prevents diffusion of gold into the substrate, thereby destroying the Schottky contact (col. 2, lines 44-51). This motivation is not specific to only GaAs substrates and would equally apply to a GaN substrate. Therefore, there is no reason why the structure of the admitted prior art cannot be modified in the manner described above. The fact that Applicants have a different reason for having a Mo layer between the other two layers is not relevant to the rejections. Applicant makes similar arguments regarding the rejections over Teraguchi in view of Nishii and Furukawa. In response to Applicant's argument that "For at least the above reasons, applicants submit that an anticipation rejection over Furukawa, which is based on GaAs FET technologies, cannot be justified", it is respectfully noted that no anticipation rejection over Furukawa was made in the Office Action. Applicant makes similar arguments regarding the rejections over Teraguchi in view of Nishii and Furukawa.

Applicant's arguments with respect to Kim (bottom of page 18 to top of page 19), filed August 25, 2005 have been fully considered and are persuasive. The rejection of claims 62-64 and 70 has been withdrawn.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew C. Landau whose telephone number is (571) 272-1731.

The examiner can normally be reached from 8:30 AM - 5:30 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should any questions arise regarding access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER

Matthew C. Landau

Examiner

November 2, 2005